REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-4 and 6-15 are currently being prosecuted. The Examiner is respectfully requested to reconsider her rejections in view of the amendment and remarks as set forth below.

Telephone Interview

Applicants note with appreciation the telephone interview conducted with Examiner Hsu on February 12, 2007. During that interview, the Examiner indicated that the current rejection could be overcome by defining the page as having memory cells within the same row since this would exclude the references which use a different array as a page. In view of the Examiner's comments, Applicants have amended each of the independent claims to now make it clear that the memory page is addressed by a row address. Accordingly, Applicants submit that the claims are now allowable.

Rejection under 35 USC 103

Claims 1-4 and 6-15 stand rejected under 35 USC 103 as being obvious over McGuinness (US Patent 6,104,416) in view of Vinekar (US Patent 5,581,310). This rejection is respectfully traversed.

The Examiner states that McGuinness shows a method of storing an array of digital data in a memory having a plurality of memory pages including the steps of dividing the array into a plurality of block units, each of the block units having a plurality of odd and even rows, and each of the rows having at least one byte. Subsequent odd rows are stored in a consecutive storage location in the first memory section and subsequent even rows are stored in the second memory section. The Examiner admits that McGuinness does not teach that one memory page has a first memory section and a second memory section.

The Examiner relies on Vinekar to teach that each bank has an odd buffer page section and an even buffer page section with the sections being on the same page. Thus, Vinekar discloses one memory page with a first memory section and a second memory section. The Examiner

feels it would have been obvious to modify the device of McGuinness so that at least one memory page has two memory sections as suggested by Vinekar.

Applicants submit that this rejection is now overcome by the amended claims. The independent claims have been amended to specifically define the memory page as being addressed by a row address. Thus, the memory has the memory cells addressed by a row address and are thus physically arranged within the same row. By describing the memory page shape, Applicant submit that the teachings of Vinekar are overcome since the description of the page in Vinekar is different.

Memory cells in a typical DRAM are physically arranged in a two dimensional array so that an individual cell is identified using a row address and a column address. Thus, memory cells within the same row are often collectively referred to as a page. For example, this definition is found in paragraph [0004] in US Published Application 2004/0155883. It is also found in column 42, lines 53-54 in US Patent 5,384,745 and in column 3, line 6 of US Patent 5,777,942. It is also found in column 3, lines 45-47 of US Patent 5,926,839.

When filing systems access data in the memory array, the system activates a "page" (all memory cells in a row) by assigning a row address to the memory. Then the system assess the data in the memory cells of the page by assigning at least one column address to the designated memory cell. Since the Vinekar patent does not indicate that the odd buffer page and the even buffer page are parts of a single page, according to the definition above, the odd buffer page and the even page in the Vinekar patent are on different pages and cannot be considered as the first memory section and second memory section according to the present claims.

The Examiner is referred to the comments in the Amendment filed August 18, 2006 for further comments regarding the operation of Vinekar patent and how the presently claimed invention is interpreted differently. Since the present Amendment further defines the meaning of the "page", Applicants submit that these comments are even more relevant.

It is further noted that the Examiner admits that McGuinness does not specifically teach a memory page having a first memory section and a second memory section. Further, Vinekar does not teach a page as presently defined having first and second memory sections. Accordingly, since the present invention describes a memory page as being addressed by a row address having

a first memory section and a second memory section and storing subsequent odd rows in a first memory section and subsequent even rows in the second memory section that the presently claimed invention is not taught be either of these references or their combination. Accordingly, Applicants submit that independent claims 1, 10 and 13 overcome this rejection.

Claims 2-4, 6-9, 11-12 and 14-15 depend from these allowable independent claims and as such are also considered to be allowable.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone of in combination. In view of this, reconsideration of the rejection and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse Reg. No. 27,295 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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